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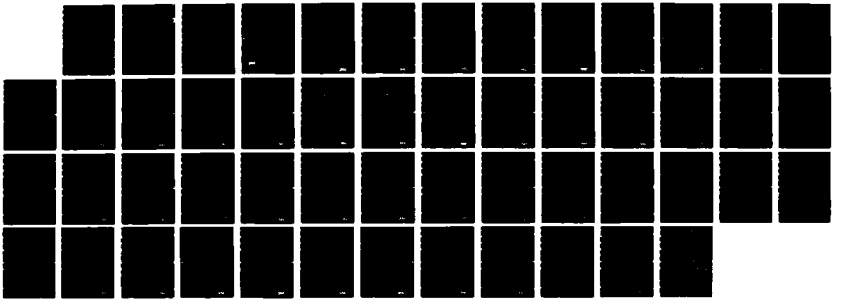

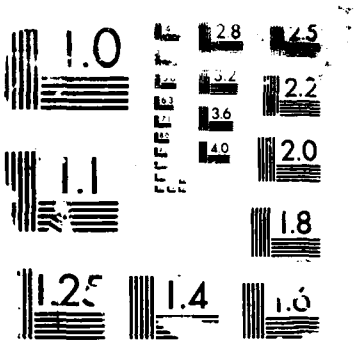
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The panelists submitted a total of 47 issue papers, which were presented for discussion at the panel meeting. Identified as high priority issues critical to a viable GaAs industry were a number related to quality material development, device physics, modeling and testing:

- There is a lack of reproducibility in bulk GaAs materials
- Methods for growth of epitaxial layers need to be developed for routine production
- Modeling of GaAs device characteristics needs substantial improvement
- There is no available test equipment with adequate speed for testing GaAs devices

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EMERGING TECHNOLOGIES PROGRAM

ET TECHNOLOGY ASSESSMENT REPORT
ET-TAR-1001

III-V MICROELECTRONICS PANEL REPORT

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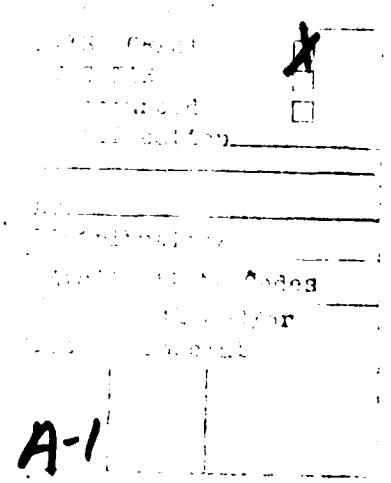
This practical constraint, inherent in technology forecasting, highlights the importance of sustaining a strong technology base program to avail of future technological changes in whatever form they appear.



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EXECUTIVE SUMMARY

The first Emerging Technologies In-Depth Assessment Panel met on November 10, 1986 to discuss III-V Microelectronics. The thirteen panelists attending included top-level technical managers from most DoD contractors in the field and two leading academic researchers. Dr. Karl Hess of University of Illinois and Dr. Dean Collins of Texas Instruments also submitted material, but were unable to attend the meeting. The meeting was chaired by Dr. Sherman Karp, a consultant intimately involved in DARPA's GaAs programs.

Panelists submitted written descriptions of significant new opportunities and problems in the field in advance of the meeting, and presented their material for discussion during the meeting. A total of 47 of these issue papers were submitted by the close of the meeting and are included in this report. Also included is a Technical Background section providing an overview of the current state of GaAs microelectronics technology.

Although the issues raised ranged from fundamental device physics to testing and system insertion, there was considerable consensus that a few of the technology issues were pre-eminent. The chairman's summary focuses on the interrelated issues of quality material development, device physics, modeling, and testing. The resolution of a number of specific problems in these areas is essential to the health of the U.S. GaAs industry. These include the lack of adequate device models, especially at the higher frequencies at which GaAs offers distinct advantages over Si, the lack of adequate test equipment both to support device modelling and to perform production testing at these higher frequencies, and the unacceptably high parameter variations in available GaAs material, both bulk and epitaxial.

The device modelling problem derives in part from the lack of measurement technology capable of collecting the data necessary to support a model, and in part from the very high frequencies (or in digital devices, short risetimes) that must be modelled as electromagnetic field interactions with active semiconductor material. The solution to the modelling problem appears to require both theoretical work and development of improved measurement technology. Models are needed to describe all current technologies: D-MESFET, E/D-MESFET, JFET, MODFET and heterojunction bipolar. There was some suggestion that supercomputers might be applicable.

The lack of adequate test and measurement equipment derives from the extreme difficulty of the problem, and the nature of the test equipment market. The problem is difficult because the devices to be measured are among the fastest devices that can be produced today. Solutions developed for Si technology are inadequate by an order of magnitude or more. The difficulty is complicated by the lack of a faster technology to be used to build the testers. Most testers today are developed by small businesses with limited resources that cannot afford to undertake development of the necessary equipment. Moreover, the current market for this equipment is extremely limited; if an adequate digital GaAs production tester were available today, domestic sales would probably not exceed ten units. This testing issue is one that probably will only be solved by government intervention.

The cause(s) of parameter variations in bulk GaAs materials is not well known, and there is some controversy as to what sources supply the best material. Some panelists felt that Sumitomo (Japan) supplied much more reproducible material than any of the domestic sources, and that part of the problem was the lack of any domestic source with the resources of Sumitomo. Others noted that they had received excellent material from Texas Instruments and Rockwell under an experimental Air Force program, but that the program was terminating and neither company had any plans to enter the business of commercially supplying GaAs material. Pilot line operators noted that a significant fraction of their cost was associated with qualifying ingots, and that the growth of longer, but not larger diameter, ingots was a priority to reduce this cost. There was a general consensus that lack of reproducible materials was a serious problem, however.

The situation with respect to expitaxial growth is also undesirable, in that the equipment and techniques for both MBE and MOCVD are complex and of a laboratory nature rather than for production. It is necessary to find or choose a technique that can be adapted to high throughput on a routine production basis (there was some sentiment that neither MBE nor MOCVD is likely to qualify). Serious investigation of epitaxial growth on foreign substrates, if successful, would provide added flexibility and possibly substantial cost savings.

In addition to the above priority issues, the panelists expressed strong interest in finding a substitute for gold metallization for contacts and interconnections and in development of suitable packaging techniques.

Problems with Au interconnection and contact metal include the lack of a selective patterning process for interconnections, and the high gamma absorption of Au that causes Au-Ga contacts to melt during gamma pulses. One panelist also noted that there was evidence that Au source and drain contacts may diffuse into FET channels, causing eventual failure of the device. Digital device manufacturers currently use lift-off for first level metal, and ion mill for second level metal patterning. The ion mill process results in high loss of yield, and consequently high cost for digital devices. An Al-based metallization is possible, and one panelist noted that Vitesse, a commercial digital GaAs startup company, plans to use an Al process to take advantage of Si processing technology. Other panelists noted, however, that the higher current densities possible in Au metallization are important for microwave devices, and that at high temperature, Al transmission lines oxidize and become lossy. Pilot line operators were reluctant to use Al for digital devices and Au for microwave, however, because current pilot line volumes are low and they desire to run both types of devices on the same lines. Panelists noted that other metals besides Au and Al might also be used.

There were also several suggestions for new directions in III-V research and development, as well as suggestions directed at facilitating insertion into systems. This panel did not interact with the formal government planning process (including the parallel deliberations of the Advisory Group on Electron Devices), except insofar as the panelists had individual personal knowledge. Therefore, specific items may overlap current or planned Government programs.

THE EMERGING TECHNOLOGIES PROGRAM

To help the Deputy Undersecretary of Defense for Research and Advanced Technology (DUSD[R&AT]) oversee investment by the Department of Defense in the technology base for development of future weapon systems, SAIC is identifying and assessing emerging technologies with potentially important military applications.

This report is one of a series under the Emerging Technologies (ET) Program. Each ET panel is tasked with identifying and assessing evolutionary changes. It is not the purpose of the ET program to attempt to predict "revolutionary" changes in technology, which by their nature cannot be predicted. This practical constraint, inherent in technology forecasting, highlights the importance of sustaining a strong technology base program to avail of future technological changes in whatever form they appear.

In the initial phases of this work, SAIC conducted a Delphi survey to identify significant emerging technologies and a workshop to examine the relative importance of likely applications of these technologies to DoD mission requirements. In the third stage of the SAIC work, panels of experts will prepare in-depth assessments of technologies that are of special interest to DUSD(R&AT) because the impact of applications of these technologies on future military capability is likely to be very broad, very profound, or both.

In consultation with the sponsor, SAIC selects teams of experts for the in-depth assessment panels who share the U.S.'s corporate knowledge of: the technology and its underlying science; U.S. and foreign programs to develop and apply the technology; and the military requirements the technology is intended to meet. SAIC selects people who work in academia, industry, and Government, but will attempt to balance panels (and instruct panelists) to avoid the biases of particular agencies, corporations, or academic institutions. SAIC suggests issues and topics to the panelists, but encourages the panelists to select approaches to their issues which suit them, and to examine additional issues and topics if this seems appropriate.

The first panel examined technologies associated with the design, fabrication, and use of electronic devices fabricated from crystals of the group III - group V semiconductors, with particular emphasis on gallium arsenide (GaAs). As discussed later in this report, GaAs integrated circuits have substantial potential advantages for both digital and analog applications. Nevertheless, transition of GaAs devices from the laboratory to quantity use in military systems has not been as rapid as might have been hoped.

This panel was assembled with the intent of providing a fresh look at the problems in GaAs IC development and manufacture, detached from detailed consideration of ongoing programs. The experts chosen for this panel are deeply involved in research and development activities on GaAs devices, so they had no need to do extensive research as a background to their panel activities.

The panel met once as a group. Prior to that meeting, each panelist was asked to submit issues important to GaAs development, with recommendations as to their solution. These issues were then discussed at the panel meeting, rewritten as appropriate, and organized into six categories by the chairman, Sherman Karp, and the SAIC panel coordinator, George Works. The chairman wrote a summary of the key technology issues, and the entire report was circulated to the panelists for their approval (and correction or change, if desired). This report is the result of that process.

CHAIRMAN'S INTRODUCTION AND SUMMARY

In the past several years, there has been an increased interest in the development of GaAs integrated circuits, for both digital and analog applications. This interest stems mainly from two important characteristics of GaAs. First, GaAs has a mobility that is several times higher than silicon, which would permit higher speed performance at lower power levels. For analog circuits this means higher frequencies of operation (through the millimeter bands) with lower front end noise figures. Second, in the absence of an oxide (i.e., except for MESFETs), the GaAs surface is stabilized by surface defect states which benefits the development of GaAs radiation-hardened circuits, since radiation-induced charging of native or deposited insulators will not cause shifts in device characteristics as it does in silicon devices.

This interest was brought into greater focus when DARPA initiated a pilot line program to increase the complexity and yield of digital GaAs circuits. Although this pilot line program has been making great strides in achieving these ends, it has also surfaced some glaring defects in the GaAs industry. These defects arise at the very basic level in the understanding of GaAs circuit development and apply equally well to analog GaAs circuits.

As an output of the Emerging Technologies In-Depth Assessment on III-V Microelectronics, a panel of experts was convened to assess the current state of the art in III-V technology, and a series of recommendations has been made which address some of the issues which stand in the way of a competitive GaAs manufacturing industry. These issues must be overcome if a reliable on-shore GaAs microelectronics industry is to be successful. Items one and two below are considered equally important and are intimately related. As such they should be considered as a priority set of issues to be addressed as one package.

1. Material Development

Many of the issues in GaAs materials are common, applying equally well to bulk or epitaxial substrates. These are availability of standard format, uniform substrates for device fabrication, good surface quality meeting physical specifications, minimal defect levels and reproducible electrical characteristics. Wafer-to-wafer and lot-to-lot reproducibility is particularly critical for pilot production of LSI devices. For ion implanted devices, issues also include the availability of sufficient regularly delivered supplies of 3 inch wafers meeting production specifications and schedules. With the startup of activities in heterostructure pilot runs, epitaxial substrates face the same requirements. Present specifications for bulk substrates include the physical requirements of surface finish, diameter, flat size, thickness, bow and taper, and orientation, and the electrical characteristics of activation of implanted dopants, resistivity before and after heat treatment, and depletion voltage at a specified temperature.

A significant amount of effort on DARPA pilot lines has been focused on wafer qualification and ingot selection. Before a boule is accepted, sample wafers undergo extensive testing. For the most part this has been due to the current lack of ingot reproducibility, which in turn stems from a lack of understanding of the relationships between the process and the resulting materials properties.

In fact it appears as though other factors besides the set growth parameters are governing the materials properties. It was the opinion of the panel that a major effort should be undertaken to fully understand the relationship between variables of the process and the parameters of the materials. The biggest crystal growth problem is retention of single crystal growth for large ingots. Focusing on using sensors to examine and control the growth interface is key here. The fundamental relationships between heat transfer, interface shape, and single crystallinity must be established in standard-type equipment. Nondestructive means of qualifying wafers at lower cost is a vital overall issue. Although the panel had varied opinions as to what specific remedies were needed, there was common agreement that the effort should be focused at one or two major ingot producers. As a minimum, this effort should: a) establish controls and procedures that will provide boule-to-boule reproducibility of "todays" high quality substrates; b) Establish methods for growth of boules that will provide at least 100 slices/boule of uniform quality at 3 inch diameter; c) conduct research to define improved growth methods that will lead to the production of higher quality substrates (yet to be defined) than are available today.

It was noted that excellent material has been developed at Rockwell and TI, under an experimental Air Force program which is soon to be terminated. Recommendations were made for the continuation of this, and a similar program, at a supplier of commercial GaAs material. This supplier would be one or more of the major vendors of GaAs wafers, selected through open competition based upon experience, cooperativeness and the willingness to "stay the course". It was felt that such an effort would be broadly supported since it would be in industry's best interest.

A second aspect of the materials growth issue was the development of high quality, reproducible, epitaxial layers for use in heterojunction devices. As in bulk growth, the growth processes in MBE and MOCVD tend to be equipment specific. The use of standard equipment for the research and development effort is essential if the results are to be transferred to the community. The critical needs for epitaxy are production quantities with reproducible characteristics. Technical issues include surface defects, growth of complex structures, equipment reliability, and spending more time growing and less time calibrating. Doping, growth rates, species flux or flow, substrate temperature, and nondestructive evaluation of characteristics are key. Defect issues are particularly acute, with the same equipment in the same laboratory operated by the same people with the same techniques showing considerable variability.

Both the equipment and techniques for MBE and MOCVD are oriented toward research and not pilot line production. Most heterostructure device research efforts even have difficulty procuring sufficient experimental substrates, not to mention their quality. The problem here is more difficult than with bulk growth, where at least the equipment is amenable to production in quantity. For GaAs epitaxy, growth equipment is fragile, with many degrees of freedom and unknowns. Fairly high level, skilled personnel are needed in the operation, maintenance and repair of the systems. In-situ sensors could help reduce the required skill level as well as improve the reproducibility situation. Batch production machines really do not exist for MBE or MOCVD. Even the very sources used in growth are in need of intensive work. MBE sources have to be refilled frequently, change properties which seriously impacts the growth processes, and still seem to fall in the 'black art' regime. Gas sources may offer hope here. However, gas sources in MOCVD have been replete with problems, most notably lack of purity and domestic sources. Particularly for complex structures with p- type dopants, the traditional MOCVD dopants

display diffusion problems. Since these devices are to be the eventual high performance digital circuits everyone has envisioned, it was felt that efforts should address: a) development of MBE or MOCVD to provide high quality, reproducible, epitaxial layers; b) development of new approaches other than MBE or MOCVD for epitaxial growth; c) development of growth of GaAs on foreign substrates with appropriate characteristics (e.g., SOS - silicon was felt to be limited in both analog and digital applications because of its high conductance).

2. Device Physics and Modeling

In concert with the development of reproducible materials is the need to provide accurate predictions of device characteristics through modeling. Unsolved problems such as backgating, short channel effects and light sensitivity are issues that will continue to plague highly integrated GaAs circuits. Accurate timing, logic and capacitance models are needed. Model work should be followed by two iterations of benchmarking with real devices to test, verify and tune the models. A realistic model for radiation effects on devices is also needed. Analog circuits lack models to predict performance accurately. This problem is exacerbated by a lack of measurement technology for data collection at higher speeds associated with GaAs technology. There are four types of testing done for GaAs devices. These are: parametric, which checks the process monitors at wafer level; probe, which checks functionality at wafer level; packaged, which checks functionality of packaged devices; and characterization, which examines the operating characteristics of the circuit.

Parametric testing is not a particular problem, except for the software development required to probe new patterns. Commercial equipment is available to do the testing task. Wafer probe capability is also available at low speeds, 10 or 20 MHz being common. The problem here, and for packaged functional test, is not only the low test speeds available, but also the pin and cost constraints. A comprehensive 256 pin tester costs several million dollars and, for the number of parts at an individual GaAs effort, may not be cost effective. None of the testers allow at-speed testing of GaAs parts. Characterization testing is generally time-intensive, with software development needed for the tests, and difficult equipment challenges in measuring short delays and performance at temperature. The primary test problems GaAs pilot lines face are access to sufficient pins, temperature testing, and at-speed measurements.

Because of the limited market projected for the high speed test equipment envisioned, it was felt that the development of such equipment would best be addressed at a center of excellence, with broad industry participation. One would envision such test equipment being constructed from either high speed GaAs heterojunction devices or even Josephson Junction devices. With the development of appropriate high speed test equipment and the availability of reproducible GaAs substrates and epitaxy, one would then expect that a device characterization and modeling effort could proceed in a predictable manner to solve the outstanding problems and develop reliable CAD software.

The recommended action is to: a) Form a center of excellence around an industry-led team to develop and implement approaches for providing high speed testing for both analog and digital ICs. The output of this effort should be a measurement system design and parts specification together with controller hardware and software that will support wafer and packaged part testing at operating levels and will accurately assess design, fabrication and assembly

performance. For digital circuits, the tester should be capable of greater than 200 pins and speeds of 1-2 GHz. The analog tester should be capable of stepping up through 100 GHz. b) Using this same center of excellence, an effort should be started in both analog and digital circuits, to consolidate the existing knowledge in device design and modeling and initiate a cooperative effort to develop the tools and models necessary for systematic computer aided design. This effort should couple with both the development of high speed test equipment and the eventual use. c) A critical part of the design and modeling process at the manufacturing level is the need to assess failure modes and provide remedial technology. Thus all major suppliers of parts should be supported to examine the failed components from their own lines. All participants must commit to complete and immediate disclosure to qualify for support. d) In addition, a study, particularly suitable for a university program, to survey the available CAD tools, their cost, equipment requirements, software language, and characteristics, would be extremely beneficial.

3. Non-Au-based Metal Contacts on GaAs

Current GaAs technology uses Au-based metallizations in fabrication. Problems with Au interconnection and contact metal include the lack of a selective patterning process for interconnections, the possible diffusion into FET channels during eutectic bonding, and low heat absorption (14 cal/g) to reach the eutectic temperature where the IC ohmic contacts will melt. The latter is of particular interest in radiation resistant devices. An Al based metallization is possible although Al oxidizes at higher temperatures causing transmission lines to exhibit higher losses. This will be of particular concern for analog devices that require higher current densities. Going to two metals (Au for analog and Al for digital) would make it difficult for concurrent use of the same pilot line for both types of circuits. Finally, the circuit use of ion mill for second level metal patterning results in high loss and, consequently, low yields resulting in higher costs for digital devices. It is recommended that a program be started to develop a global wiring scheme for advanced designs in GaAs, which would create Si-type fabrication techniques for GaAs ICs and increase compatibility between GaAs and Si wafer fabrication and design technology.

4. High Speed Packaging for Digital and Analog Circuits

In the frequency range from 20 to 50 MHz on digital circuit boards, a major change occurs in the electrical characteristics of existing packages. Consequently, as GaAs chips are designed with over two hundred connections operating at speeds of 50-220 MHz, these existing packages will become limiting and put a cap on the performance of GaAs digital circuits. In analog GaAs, the situation is even more serious, with very expensive, labor-intensive fixturing required for these circuits. Both types of packages need to be developed. The first being the development of high speed packaging techniques which are compatible with the projected needs of digital GaAs circuits. The second involves a need to focus on packages for MMIC testing, and MMIC final assembly.

5. New Research and Development

Naturally, many suggestions for new directions in III-V development were also submitted, and they are also enclosed in this document. These will not be elaborated upon, except to note that there are very few other areas where funding for these ideas can be obtained, yet they will be needed in the future for a world-class GaAs industry.

TECHNICAL BACKGROUND

Due to their unique properties, III-V compound semiconductors, in particular GaAs, are the subject of intense interest for microelectronics. Electron velocities up to five times faster than silicon provide GaAs with a higher speed capability in digital integrated circuits (ICs), achievable with lower power dissipation. Frequency ranges not accessible with silicon can be addressed with GaAs microwave and millimeter wave devices. Wide temperature ranges (± 200 degrees) are possible with appropriately designed and fabricated compound semiconductors. Exceptional radiation hardness, i.e., total dose performance two orders of magnitude better than silicon, has also been demonstrated with GaAs devices.

These factors account for the growing importance of compound semiconductor technology for applications such as communications, computing, signal processing, instrumentation, and radar, especially for military and space applications. In research facilities around the world, GaAs and related compounds are under investigation, to bring the high performance promise of the technology into reality. However, the challenges to moving an emerging GaAs technology to system readiness are very considerable. Realistic assessment of the potential, status, and problems, together with well-planned and managed programs to address these, are critical for the United States to capitalize on this opportunity, and maintain on-shore sources for this technology.

In the late 1960's, activity in compound semiconductors moved from investigation of materials and properties into the device regime. By the 1970's, simple GaAs digital and microwave devices were being demonstrated which showed great promise, but were plagued with serious problems due to the embryonic state of the materials, processing, and design technology. In the 1980's, the development of ion implantation techniques and growth methodology for liquid encapsulated Czochralski (LEC) pulled GaAs materials thrust GaAs ahead of the other compound semiconductors and into accelerated development.

Previous to these events, progress had been severely limited by the lack of an effective means to form active layers in GaAs, other than by epitaxial techniques such as vapor phase epitaxy (VPE). These early epitaxial substrates, with their size and quality limitations, did not support complex integrated circuit structure formation. Diffusion methods were also generally unsuccessful in GaAs, due to decomposition of the substrates at high temperatures.

The development of ion implantation and annealing techniques provided GaAs with the same advantages that these methods provided silicon - controllable, selective doping across the wafer surface. However, the early GaAs substrates grown in quartz tubes in furnaces by the gradient freeze method suffered from a variety of problems, including variable, irregular size, lack or loss of insulating characteristics, high background impurity levels, gradients in electrical properties across wafers and through ingots, physical defects such as inclusions and voids, and poor surface finish.

The evolution of LEC materials, pulled and finished like silicon, brought the availability of standard format round wafers, higher yields of semi-insulating ingots, and more uniform electrical properties with fewer gross defects. This allowed GaAs to capitalize on the developments in silicon technology and use standard processing equipment. In turn, the startup of pilot production operations became viable. By the 1980's, several pilot production facilities for the manufacturing

of digital and microwave circuits were underway, utilizing ion implanted device structures. The two DARPA pilot lines were started and LSI (large scale integration) devices were demonstrated at several facilities. Activity in the compound semiconductor research community began to shift into the development of devices based on advanced epitaxial techniques for even higher performance characteristics.

While sufficient to begin pilot production activities, many of the basic supporting technology areas continue to be characterized by serious, unsolved issues. These include materials quality and availability, the qualification of suitable materials, high yielding process techniques, metalizations for contacts and interconnects, reliability and failure analysis, assembly methods, computer aided design and modeling support. While considerable carryover from significant investments in silicon technology has benefited GaAs development, many facets unique to the emerging compound semiconductors remain to be addressed.

The advanced compound semiconductor epitaxial approaches, which are now garnering the largest share of research and development attention, build on the foundation of the ion implanted pilot production technologies. The critical issues are frequently common, with the same barriers inhibiting progress in both the ion implanted and epitaxial device families.

A number of different GaAs device technologies presently exist in differing stages of evolution, suitable for various device types and specifications. The most mature of these, using ion implantation into semi-insulating GaAs substrates, are the D-MESFET (depletion metal semiconductor field effect transistor) and the JFET (junction field effect transistor). These are the technologies in use in the first and second DARPA (Defense Advanced Research Projects Agency) pilot line programs for the development of production capabilities of LSI circuits such as 16K RAMs and 6K gate arrays. The D-MESFET is also the dominant commercial approach for GaAs integrated circuits for both digital and microwave devices. Selected 1-3 GHz MSI (mdeium scale integration) level GaAs ICs are offered commercially. Several laboratories have demonstrated GaAs LSI prototypes, including fully functional 4K RAMs and 6K gate arrays specialized with 12 x 12 multipliers.

D-MESFETs (Figure 1) are "normally on" devices, i.e., current can normally flow through the channel under the gate. A negative potential on the gate causes the gate to "pinch-off" or deplete the carriers in the channel, stop the current flow, and turn the device off. This "pinch-off" or threshold voltage is generally 0.5 to 2.5 volts, with microwave device thresholds higher than digital. A shallow n- ion implant is used to form the active channel layer, with a deeper n+ implant for the source and drain regions. Photoresist is used for masking, so that selected, isolated regions can be doped by ion implantation.

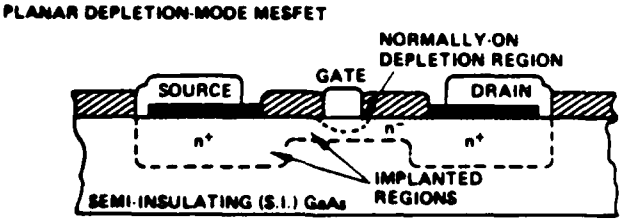

Figure 1

The ohmic contacts for the source and drain are separated by only several microns, usually with a 1 micron long Schottky barrier gate located in between. Typically, AuGe (gold-germanium) ohmic and TiPtAu (titanium-platinum-gold) Schottky contact metalizations are used. These first level interconnects are defined by a lift-off technique, in which a wafer with patterned photoresist is covered with evaporated metal and then soaked in or sprayed with a solvent. The metal adheres where the bare wafer was exposed, but floats away with the photoresist where metal was on top of this film. Optical lithography techniques are used for patterning the light-sensitive photoresist. For microwave devices, electron beam lithography is frequently used to form a submicron gate structure. Dry etching techniques, using energized gas atoms to erode layers of dielectric or metal through openings in the patterned photoresist layers, create the integrated circuit features. A second level interconnect is typically TiAu (titanium-gold), e.g., for running power buses in the circuit. After deposition of a protective overcoat and opening holes in this film to expose the bonding pads, devices are mounted in packages, generally using conductive epoxy, and wire bonded and lid sealed.

Devices are typically tested for: parametrics - examination of test structures to assess process control; functional probe-determination of the functional yield of die on the wafer; and packaged test - verification of functionality after assembly. A new circuit also undergoes intensive characterization testing to determine speed, power consumption, operating supply range, and reliability. In general, test equipment developed for silicon technology adequately serves digital GaAs testing. High speed testing is still a considerable challenge, however, and frequently limited to characterization due to the equipment limitations. High speed production testing of GaAs is not yet viable. GaAs chips for testing other GaAs chips, and on-chip testability are being investigated to fill this gap. Microwave chips present even more complex testing considerations. These are generally tested for parametrics, examined using special probes if they are low frequency (under 20 GHz), and characterized after mounting in a fixture.

A variety of logic design approaches are used for D-MESFET circuits. These include BFL (buffered FET logic), SDFL (Schottky diode FET logic), CCFL (capacitor coupled FET logic) and SCL (source coupled logic). Circuits generally use two power supplies plus internal level shifting in operation. Computer aided design techniques developed for silicon ICs are used for simulation, layout, capture, and checking. Models and worst case files describing production tolerances based on measurements of GaAs devices and test structures are used as the basis for design and model calculations.

While this is the most mature GaAs integrated circuit approach, offering the promise for system parts within the next several years, serious basic technical challenges remain for this emerging technology to reach a capability for LSI parts meeting system specifications. These challenges range from quality and supply of GaAs substrate materials, through fabrication and packaging issues, to accurate device models for circuit design. Considerable progress has been made in the past five years as a result of DoD and industrial programs. However, the state of the technology is not comparable to commercial silicon, despite the potential performance advantages.

The D-MESFET technology can support high speed digital circuit operation with moderate-to-low power dissipation. Generally, speed and power are linked in a trade-off relationship, connected also with yield. Higher speeds usually involve higher power consumption, although higher in this case is considerably less than comparable silicon circuits. Higher performance

frequently involves designing around tighter device parameters, requiring better control of the fabrication process and electrical characteristics. Lack of this control can result in the devices not working correctly or decreases in circuit yield. The D-MESFET approach is also successfully utilized for microwave applications at the low frequency end, including low noise devices. Combined with other GaAs devices, the D-MESFET digital technology has been combined with optoelectronic and microwave components to demonstrate "system on a chip" prototypes.

The D-MESFET technology is being used to fabricate 16K RAMs and 7K gate array prototypes in pilot production with DARPA support. However, with these circuits, the D-MESFET is approaching its complexity limit pending the development of additional layers of global metal wiring and special measures for heat dissipation. The circuits at these levels of complexity fill a lithographic exposure field. Large chips also suffer from yield reduction affected by defects per unit area.

A more recently developed technology family, the E-MESFET (enhancement MESFET) technology (Figure 2) offers potentially dramatic advantages over the D-MESFET in chip size and performance, while maintaining the same general fabrication approach using ion implantation into semi-insulating substrates. The E-MESFET uses the built-in potential of the Schottky barrier to completely "pinch-off" or deplete the channel. It is thus a "normally off" device. The E-MESFET utilizes a lower positive threshold voltage (<0.5 volt) to allow conduction through the channel between the source and drain to turn the device on.

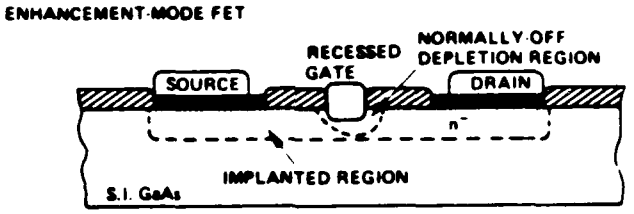

Figure 2

Control of the threshold voltage value and its variation requires a much tighter control of the fabrication process than for D-MESFETs. Recessing by etching the area under the gate is used to control the threshold voltage value and reduce source resistance. High source resistance, which degrades the device transconductance and, thus, the speed, is a problem resulting from a depletion region at the GaAs surface tending to "pinch-off" the lightly doped channel. Self-aligned structures are under development in many laboratories, to use the gate metalization as a mask to define the source and drain implants for improved conductivity. This allows closer placement of the source and drain to the gate than achievable by normal lithography. Other than these variations, the E-MESFET is fabricated in the same way as a D-MESFET.

Typically, a DCFL (direct coupled FET logic) approach is utilized for enhancement circuits, which requires only a single power supply. For additional drive capability and noise

margin, other types of logic may be combined with DCFL, requiring an additional power supply. Frequently, enhancement and depletion elements are required to perform a given logic function using the enhancement approach, allowing as much as a 40% reduction in circuit area, or the fabrication of more complex chips. The applicability of NMOS silicon circuit approaches to the E/D-MESFET technology is another significant advantage.

Higher speeds (greater than 4 GHz) and transconductances have been demonstrated by E-MESFETs than with D-MESFETs. Combined with the area and power supply considerations, the enhancement MESFET is a highly desirable GaAs technology approach. This technology is, however, very challenging to fabricate with sufficient control to maintain the required circuit noise margins. The most complex devices, 16K RAMs and 16 x 16 multipliers, have been demonstrated in Japan.

Another family of enhancement-mode circuits is the JFET (junction field effect transistor). Less commonly used, this technology (Figure 3) uses ion implantation to place a n-p junction underneath the gate. This structure minimizes the high series resistance for a "normally off" device channel. Selection of the p implant energy allows adjustment of the appropriate threshold voltage, after initial measurement of the lightly doped n- channel. Other fabrication steps for JFETs are very similar to those for MESFETs.

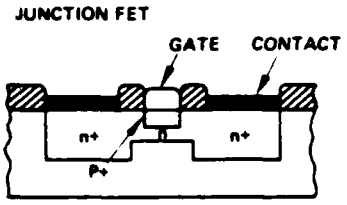

Figure 3

J-FETs offer very low power circuit operation and impressive radiation hardness. They do, however, occupy larger circuit areas and operate at lower speeds than MESFETs. The latter is a result of the lower observed transconductances. LSI circuits have been demonstrated in the J-FET technology, including 4K RAMs under DARPA pilot line support, and 1500 gate arrays.

The aforementioned GaAs device technologies all utilize ion implantation into semi-insulating substrates to form the active device layers. New generations of research devices are based on heterojunctions, layers of specially tailored compound semiconductor films grown on a substrate, typically GaAs. Research techniques such as molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD), sometimes referred to as metalorganic vapor phase epitaxy (MOVPE), are used to deposit precisely controlled, very thin (tens of Angstroms) films in sophisticated very high vacuum systems. These heterojunction devices offer even more exciting prospects for higher performance, but they are significantly more difficult in regard to materials, fabrication, testing, design and modeling.

The most straightforward of these technologies is the HEMT (high electron mobility

transitor), also called the MODFET (modulation doped field effect transistor) or TEGFET (two-dimensional electron gas field effect transistor). HEMT structures (Figure 4) utilize a metal gate over a thin layer of aluminum gallium arsenide (AlGaAs) grown over a layer of undoped GaAs to form a field effect transistor. Isolation between elements is formed by ion implant damage. The rest of the device processing is quite similar to that of a MESFET.

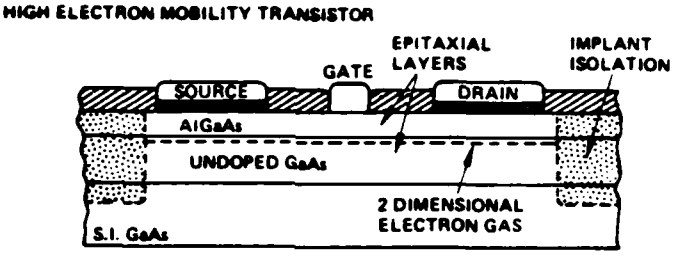

Figure 4

Very high electron mobilities result in HEMT structures when the carriers flow from the AlGaAs layer into the undoped GaAs layer. Even higher channel mobilities result at low temperatures, when scattering decreases in these undoped layers. An order of magnitude greater channel mobility than MESFETs is observed for these HEMTs, with high transconductance. The result is significantly higher switching speeds and improved gain bandwidth products.

Both enhancement and depletion FET design and fabrication technology can be utilized for HEMT devices. Compared to E/D-MESFETs, higher speeds can be attained with lower power dissipation; this has been demonstrated in 1k and 4k RAMs. Of particular interest is the application of HEMT technology to low noise millimeter wave devices. However, questions remain at present in regard to the radiation hardness, reliability, and manufacturability of these circuits. Since MBE and MOCVD are largely research tools at present, intensive effort remains to address the volume production of reproducible, defect free layers on standard wafer sizes for HEMT.

Another heterojunction technology offering the potential for possibly the highest achievable speeds in compound semiconductor digital devices and high frequency millimeter wave devices is the heterojunction bipolar transistor (HBT or HJBT). HBTs also utilize epitaxial substrates. More complex than HEMT structures, HBTs can be fabricated either emitter up

(Figure 5), for ECL circuit applications, or emitter down, for I2L applications. The threshold voltage is controlled by the channel doping and layer thickness of the epitaxy. The emitter has a wide band gap enabling high base doping in a very thin layer. This results in gain-bandwidth products potentially greater than 100 GHz. Values in the tens of gigahertz have already been observed.

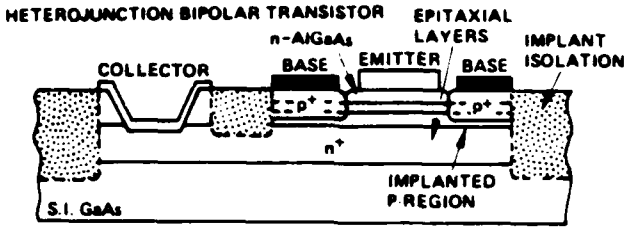

Figure 5

The HBT layered structure is complicated, requiring a series of precision growth steps to produce the epitaxial layers. MBE has been used for the ECL HBT approach, however, MOCVD is being successfully utilized for I2L circuit fabrication. With its potential for high throughput batch processing, MOCVD is regarded as the most practical approach for manufacturing quantities. Since both n and p type layers are involved, ion implantation and contact formation issues are more difficult than for MESFETs or HEMTs. Self-alignment techniques are under investigation for one micron or less gate widths.

The HBT offers not only the potential for outstanding speed performance, but also excellent drive capability. HBTs are particularly well suited to the fabrication of gate arrays and also A/D (analog to digital) converters. The power consumption of typical HBT devices is, however, quite high compared to other GaAs technologies. To date, the circuit areas occupied are relatively large compared to other GaAs technologies. Excellent radiation immunity has been documented for HBT devices. Both the ECL and I2L approaches have produced fully functional circuits. The ECL approach has produced higher frequency operation in MSI devices than the I2L technology. More complex circuits such as 6K gate arrays have been produced using the I2L approach.

While these and other compound semiconductor device technologies are at varying stages of maturity, they face many of the same challenges. The newly emerging technologies will not necessarily supplant the more mature approaches, since the unique features of the system application will dictate the optimum technology choice. The transition from a research concept to a qualified device meeting specifications acceptable for system insertion is an awesome challenge for a new technology. Yet, the potential payoff for this investment, in terms of performance, compound semiconductor development is considerable, particularly for DoD applications.

The panel members assembled for the III-V Microelectronics Panel of the Emerging Technologies Program are intimately aware of these formidable challenges through first hand experience in research, development, and pilot production in GaAs and other compound semiconductors. The panel's recommendations reflect that perspective to accelerate and secure the position of GaAs technology in the United States, assuring its availability to DoD.

MATERIALS ISSUES: SUBSTRATES AND EPITAXY

TITLE	AUTHOR
Bulk Materials Properties Control	T. A. Midford
Qualification of LEC Material for LSI	G. L. Troeger
Material Research for High Yield IC Processing	R. Zuleeg
Controlling As Inclusions in GaAs	W.E. Spicer
Materials Growth for GaAs Devices	C. G. Kirkpatrick
Size and Quality of GaAs Substrates	S. H. Wemple
GaAs Growth on Foreign Substrates	R. W. Bierig
GaAs/Si	J.S. Harris
High Throughput, High Precision Epitaxy	T. A. Midford
High Throughput Epitaxial Growth of Heterostructures	C.T. Roberts
Active Layer Formation for High Yield	S. H. Wemple
Selective Epitaxy	R. W. Bierig

MATERIALS: SUBSTRATES AND EPITAXY

Issue: Bulk Materials Properties Control **Submitted By:** T. A. Midford

Description: Bulk materials properties and the relative lack of control over them are frequently cited as causes for the low functional yield (with intolerable performance limits) of GaAs discrete devices and ICs. Despite the frequency of this observation, the relationship between most material parameters and specific aspects of device performance is poorly understood. Detailed studies which establish definitive correlation between materials properties and device performance are lacking at present. Much of the reason for the lack of data lies in the cost of fabricating and measuring large quantities of diagnostic test patterns necessary to establish correlation between starting material properties and device results.

Recommendation: A meaningful program would attempt to document relationships between materials properties and device performance. Extensive initial measurements of the starting material would be made prior to device fabrication with a standard process. Subsequently, measurements on devices would be used to provide data which could be correlated with starting materials properties. A wide variety of initial materials tests would be required since the materials-device relationship is not known a priori.

Benefits: Better understanding of the device materials relationship would permit increased yield, thereby, lowering the cost of the final circuits. Higher yield would raise the affordable number of elements per system, or in some cases, make new monolithic approaches fall within an acceptable cost range.

Issue: Qualification of LEC Material for LSI **Submitted By:** G. L. Troeger (via R. Zuleeg)

Description: Material variations from slice to slice, ingot to ingot, and vendor to vendor are causing unacceptable variations in device parameters for LSI and VLSI circuit fabrication. Causes of the variations can often be traced to changes in EL2 concentrations, subsurface damage from sawing and polishing, EPD, shallow and midgap impurity concentrations, and stoichiometry. In addition, the response of the wafers to cleaning, capping, implanting, annealing and contacting procedures varies depending on the process, making duplication of results difficult in separate labs.

Recommendation: Study the causes of the variations in terms of parameters that both growers and users can measure or control.

Benefits: Improved yield for high speed, low power, and radiation hard GaAs ICs.

Issue: Material Research for High Yield IC Processing **Submitted By:** R. Zuleeg

Description: The promises of semi-insulating GaAs for high yield IC processing can only materialize when uniformity of threshold voltage requirements across a wafer and the isolation resistance values for closely spaced IC components can be met. Indium doping is a remedy for threshold voltage control and proton bombardment or ion implantation of boron is a temporary solution to avoid the isolation problem.

Recommendation: Material analysis by DLTS, PIS, Hall-Effect, SIMS, ESCA, PL and DC measurements are proposed to identify and qualify LEC GaAs material for its properties of threshold voltage control and isolation resistance. In cooperation with material suppliers, controlled processing techniques should be established to guarantee qualified material for pilot line operation of LSI and VLSI GaAs circuits for DoD needs.

Benefits: Would make pilot line operation more profitable in the production of GaAs ICs for military and space applications.

Issue: Controlling As Inclusions in GaAs **Submitted By:** W.E. Spicer

Description: Work on GaAs has been plagued by materials problems. For example, reproducibility and stability of semi-insulating GaAs and of ICs fabricated on such material is a problem. (This is closely interrelated with such problems as dislocation counts in this material). The As anti-site defect is most often associated with the EL-2 center producing semi-insulating GaAs. There is other strong evidence of excess As being present in GaAs. For example, the Optoelectronic Joint Laboratory (OJL) has evidence for non-electrically active interstitial As at the 10^{17} to $10^{18}/cm^3$ level. They believe this produces As anti-site defects. Others have found evidence of As inclusions in GaAs. Until the inclusion of excess As in GaAs and its effect on ICs and IC processing is understood and controlled, difficulties may be expected in production of GaAs ICs and other device structures.

Recommendation: To understand the inclusion of As in GaAs and its effect on the properties of ICs and other GaAs device structures. It is critical that such a program be closely related to other programs such as those to reduce dislocations in GaAs. The overall objective is: 1) to understand the effect of As excess on GaAs properties and, in particular, on the electrical properties of device structures fabricated in GaAs; 2) to learn to control and obtain optimum amounts of As in GaAs; and 3) to improve reproducibility, stability, and production yield for ICs and other device systems fabricated in GaAs.

Benefits: Better ICs and other device structures fabricated in GaAs with increased stability and reliability. Decreased costs due to higher yields.

Issue: Materials Growth for GaAs Devices **Submitted By:** C. G. Kirkpatrick

Description: While the materials for GaAs devices have improved significantly with the development of semi-insulating LEC materials, issues remain which limit the progress in digital and analog integrated circuits. These issues involve the limited length of ingots, which is serious due to the extensive qualification now requiring process capability to determine if ingots are usable. The cost and effort of qualification on a per ingot basis would be reduced by larger wafer counts per ingot. Improved quality control of the physical and electrical characteristics is still a serious issue. Variability in vendor control of wafer size, flat size, surface finish, and flatness, as well as considerable variability in the activation characteristics in uniformity and reproducibility are all too common. Those supporting DoD programs and attempting to develop on-shore sources of materials find the domestic sources particularly deficient.

Recommendation: Program objectives should involve improved quality control of 3-inch LEC materials. Both physical and electrical characteristics should be addressed.

Benefits: Benefits accruing to DoD from such a program would be reduced cost in the fabrication of GaAs devices and improved yields and performance of GaAs devices.

Issue: Size and Quality of GaAs Substrates **Submitted By:** S. H. Wemple

Description: The throughput and cost of ICs depend to a significant degree on wafer size and quality. Expansion beyond 3" in the future may be mandatory if LSI/VLSI is to achieve high volume manufacture.

Recommendation: Expanded developments for 4" GaAs and $\geq$ 4" GaAs on Si. Program should include not only crystal growth, but also wafer handling and wafer preparation techniques including polishing and cleanliness issues.

Benefits: Higher volume, lower cost digital and analog ICs.

Issue: GaAs Growth on Foreign Substrates **Submitted By:** R. W. Bierig

Description: Deposition of high quality GaAs on insulating substrates (not GaAs) will support a number of opportunities noted below. The substrate properties that are desired are low electrical conductance, low preparation cost, large bandgap (high temperature stability), high thermal conductance, low loss over the frequency range 1-100 GHz, and mechanical stability. Success in this effort could make significant impact on the position now held by the Japanese in GaAs semi-insulating substrate supply and not only make the U.S. self-sufficient, but a leading

world supplier. Current work to grow GaAs on silicon will not solve the problem. Silicon's low band gap (~1 ev) and relatively high conductance (~1000 Ω -cm) limit applicability. Of particular value will be substrate materials with very high thermal conductance since such material has the potential to significantly expand GaAs power FET performance.

Recommendation: A four Phase Program is recommended. Phase 1 (1 year): Construct a matrix of known materials with properties matching requirements. Submit data to scrutiny of expert panel at 6 months and 12 months. Select no more than two material types for development. Phase 2 (12 months): Use existing GaAs growth methods (MOCVD, MBE, LPE, VPE, etc.) to evaluate feasibility of success. Evaluation to be made both experimentally and theoretically. Output of Phase 2 is Phase 3 plan. Phase 3 (3 years): Develop high quality epitaxial growth and technology plan - Phase 4: Technology Implementation - 2 years (1 year concurrent with Phase 3). Estimated Program cost: Phase 1, $150K; Phase 2, $300K-500K; Phase 3, $3M; Phase 4, $2M; Total ~ $6M.

Benefits: GaAs material base compatible with optical, digital, microwave and mm wave device and circuit development. Improved power dissipation in GaAs FETs and circuits. A medium that will support implementation of a low cost (one surface) fabrication process. Elimination of dependence on foreign supply.

Issue: GaAs/Si **Submitted By:** J. S. Harris

Description: GaAs/Si has hit with very surprising success and could have a major impact on high speed IC technology. Because of the surprising success, there has been little thought into research beyond the materials research and initial device demonstrations. There are still many unknowns in the materials technology, but initial investigation of application this technology appears warranted at this time. The potential for 4" or 6" GaAs/Si is probably much better for this than bulk GaAs because of thermal constraints in bulk growth and fragility of large GaAs wafers.

Recommendation: Investigate GaAs IC fabrication on GaAs/Si. Investigate growth for 4" and 6" GaAs/Si.

Benefits: Could combine advantages of optical and high speed GaAs with high density and low power of Si (particularly CMOS). Large area GaAs/Si may be achieved much better than large area bulk growth approach.

Issue: High Throughput, High Precision Epitaxy **Submitted By:** T. A. Midford

Description: Advanced high performance III-V microelectronics will require high precision, reproducible and eventually high throughput epitaxy for the fabrication of heterojunction based devices. Until now, R&D device structures have been based almost entirely on molecular beam epitaxy (MBE) and, very recently, on metal organic vapor phase epitaxy (MOVPE). MBE provides the greatest degree of precision and flexibility, but is severely limited in throughput. MOVPE has the potential for high throughput on 3-inch diameter or larger wafers but this has not yet been verified. In addition, there are, at present, both government and company funded R&D programs dealing with hybrid technologies incorporating some features of both MBE and MOVPE and which are aimed at higher throughputs.

Recommendation: Define and develop one or more high throughput III-V epitaxial technologies, suitable for the growth of advanced device structures including heterojunctions, high electron mobility transistors (HEMT), heterojunction bipolar transistors and superlattices. Throughput objective: fifty 3-inch or larger diameter wafers per day. Develop the required equipment and validate by the high rate production of material to be used for device fabrication in one or more existing process lines.

Benefits: Establish source(s) of material for a wide variety of RF and digital devices and integrated circuits.

Issue: High Throughput Epitaxial Growth of Heterostructures **Submitted By:** C.T. Roberts

Description: Rapid progress is being made on high performance circuits based on MODFET devices. However, the technology for low cost preparation of heterostructures does not exist. The layer properties (perfection, thickness, uniformity and doping level tolerances) are very critical. Increased effort on low cost, high volume epitaxial growth methods is required.

Recommendations: Develop new approaches for epitaxial growth of III-V materials that are clearly capable of meeting requirements for MODFET devices and high throughput, low cost production. MBE and MOCVD are excluded.

Benefits: Provides technology to make heterostructure devices available at low cost for DoD systems.

Issue: Active Layer Formation For High Yield **Submitted By:** S. H. Wemple

Description: The problem of device parameter control strongly impacts circuit yield. Structures formed by MBE or MOCVD could be explored with the specific goal of improving yields rather than generating extraordinary electrical characteristics.

Recommendation: Modeling and epi structure optimization for maximum circuit yields.

Benefits: Lower cost products.

Issue: Selective Epitaxy **Submitted By:** R. W. Bierig

Description: Device and component integration is optimally performed when localized doping can be provided to support optimization of device properties. An example is an MMIC T/R module used in an array with fiber optic command/control communication. In fully integrated form device types to support low noise amplification, power amplification, switching; optical modulation, optical generation and optical detection would be required. With significant performance compromise, most of the device types can be implemented by direct ion implantation into semi-insulating GaAs. In the long-term, high quality performance and multi-function integration can possibly be realized more inexpensively by selective epitaxial growth. The potential cost/benefit leverage for such technology is huge in terms of reduction of assembly/test cost.

Recommendation: Demonstrate feasibility of growing epitaxial structures to support MESFETs, HEMTs, LEDs, lasers, and optical modulator/detectors in a single chip structure over at least 80% of a 3" diameter substrate. This program should be coordinated with a program of growth on foreign substrates. Three Phase program: Phase I, program plan and approach evaluation/6-12 mo, $100K - $150K; Phase II, two competing contracts/2 years duration, $350K - $500K/year/contract; Phase III, one contract to optimize growth and integration demo/3 years, $3M. Total program duration is 5-6 years; total cost is $4.5M - $5.2M.

Benefits: Major cost reduction in multi-function assemblies; performance optimization of devices in highly integrated components.

DESIGN AND MODELING ISSUES

TITLE	AUTHOR
Device Physics Issues in GaAs ICs	C. G. Kirkpatrick
CAD and Modeling for Millimeter Wave Devices and Integrated Circuits	T. A. Midford
Supercomputing - Device Modeling	K. Hess
Design and Modeling Tools for GaAs	C. G. Kirkpatrick
Design Methodology	C. G. Kirkpatrick
Chip Design Architecture and Logic Families for the Highest Speeds	S. H. Wemple

DESIGN AND MODELING

Issue: Device Physics Issues in GaAs ICs **Submitted By:** C. G. Kirkpatrick

Description: Problems in device physics of GaAs such as understanding backgating, short channel effects, light sensitivity, and other phenomena still remain as issues. Understanding of these is critical to achieving the device performance offered by GaAs.

Recommendation: The program objective should focus on understanding basic device physics problems in GaAs ICs, with particular emphasis on backgating - its cause, its effect, and its cure.

Benefits: The benefit to DoD will involve improved device performance of GaAs devices.

Issue: CAD And Modeling For Millimeter Wave Devices And Integrated Circuits **Submitted By:** T. A. Midford

Description: Currently there are almost no tools and models for the systematic computer-aided design (CAD) of millimeter wave devices and integrated circuits (MMICs). Design of millimeter wave MMICs is largely empirical and usually requires several iterations of design, fabrication and test to achieve acceptable levels of performance. There is a deficiency in both active device and circuit models which is compounded by a lack of automated and well calibrated millimeter wave test equipment. Over the long term, the further development, as well as the efficient utilization of this emerging technology, will be seriously limited by these design tool deficiencies.

Recommendation: Define a unified approach to the development of millimeter CAD methodology. Where possible, draw from the extensive experience gained at microwave frequencies in the design of MMIC devices. Develop and verify circuit element and active device models leading to the equivalent of a cell library. Implement the entire system on commercial hardware.

Benefits: This work will make possible the cost effective development of millimeter wave MMIC devices.

Issue: Supercomputing - Device Modeling **Submitted By:** K. Hess

Description: III-V compound devices are more difficult to model than silicon devices and require large computational resources because of the complicated equation of motion for the electrons. Reliable tools for computer aided engineering are needed for digital applications and especially for microwave device applications above 40 GHz.

Recommendation: Development of computer aided engineering tools for the design of III-V compound field effect transistors in two stages: Rigorous physical models implemented in Monte

Carlo simulations with quantum corrections and subsequent use (in form of look up tables) of these results in simple simulations which account for complicated device geometry, etc.

Benefits: Ultrahigh speed FETs.

Issue: Design and Modeling Tools for GaAs **Submitted By:** C. G. Kirkpatrick

Description: In order to provide high performance, error-free designs in GaAs digital and analog devices, improved CAD tools and models are needed. The problem is deeper than software development, since actual production run data and benchmarking of designs to verify the accuracy of models and tools are required. The payoff is significant, in reduced cost of designs with greater likelihood of first pass success, and in the performance meeting design goals. The situation for analog devices is even more serious than for digital, with the design tools still embryonic. For digital, piggy-backing on silicon developments has capitalized on existing tools for GaAs design.

Recommendation: The program objective should be to develop a sufficient data base for design rule and model information, develop models for insertion into non-proprietary software such as SPICE, and use this information to design circuits for benchmarking. This benchmarking would verify the accuracy of the tools and delineate further issues to be worked.

Benefits: The benefits to DoD would be multiple. The ability to rapidly and accurately design into GaAs technologies would facilitate the development of real products rather than prototypes. The cost of developing circuits would be reduced through improved accuracy and achieving performance requirements without repeated iterations of actually making the device.

Issue: Design Methodology **Submitted By:** C. G. Kirkpatrick

Description: A considerable investment has been made by the commercial and DoD community in the development of silicon-based design methodology. The application of this technology, standard cell methodology, design rule checks, netlist checks, model and simulation tools, and logic family development, should be thoroughly investigated for GaAs.

Recommendation: The program objective should be the identification of Si design methodology transferable, or suitable for application with minimum modification, to GaAs design tasks. The transfer across technology lines, Si bipolar to GaAs bipolar, Si NMOS to GaAs E/D, should be investigated.

Benefits: The benefit to DoD is substantially enhanced design capability in GaAs with minimum investment in cost and cycle time.

Issue: Chip Design Architecture and Logic Families for the Highest Speeds

Submitted By: S. H. Wemple

Description: Digital circuit performance depends critically on internal logic delays and the number of delays per logic function. Optimization may depend on the logic family chosen, the presence of Schottky forward conduction, the availability of on-chip resistors, power supply choices, etc.

Recommendation: Investigate design strategy for the highest performance taking into account device characterization, logic families, yields, and internal architectures. The latter may include the standard cell library approach.

Benefits: Higher performance circuits.

PROCESSING TECHNOLOGY ISSUES

TITLE	AUTHOR
Metallization Schemes for GaAs Circuits	C. G. Kirkpatrick
Metal Contacts on GaAs	W. E. Spicer
Non-Au-Based Metallizations	S. H. Wemple
Al-Metallization to Replace Au	R. Zuleeg
Interconnect Capacitance Reduction	S. H. Wemple
Low Cost FET/MIMIC Technology	R. W. Bierig
HIgh Throughput Sub-Half-Micron Lithography	T. A. Midford
In-Situ Processing for High Performance GaAs Devices	J. S. Harris
Packaging for GaAs Digital and Analog Circuits	C. G. Kirkpatrick

PROCESSING TECHNOLOGY

Issue: Metallization Schemes for GaAs Circuits **Submitted By:** C. G. Kirkpatrick

Description: The addition of metallization schemes should allow the application of more advanced designs in GaAs as in silicon through the use of global wiring. The techniques for these interconnect systems, the metals to be used, and the layout rules for their usage, are undeveloped at present for GaAs.

Recommendation: The program objective should be the development of global wiring schemes for advanced circuit designs in GaAs.

Benefits: The benefits to DoD from such a program would be smaller, more powerful chips with higher yields, emulating silicon functions with higher performance.

Issue: Metal Contacts on GaAs **Submitted By:** W. E. Spicer

Description: There are potential problems with metal contacts on GaAs which could, for example, limit production yield as advanced GaAs ICs are put into production. Perhaps of most pressing concern are "ohmic" (i.e., low specific resistance) contacts; however, Schottky barrier (i.e., rectifying) contacts also present potential difficulties. Contact problems can be conveniently placed into two general categories: electrical characteristics and dimensional issues. High specific resistance of a contact or variation in Schottky barrier height may limit unacceptably the electrical performance of a device. Changes in these parameters may be due to such factors as processing or operating temperatures from surface conditions prior to metal deposition, leading to unacceptable variation in IC operating parameters. An important aspect is the chemical reactions which take place between deposited metals and GaAs. In addition to changing electrical properties, these can lead to changes in device dimensions which can be critical for close spaced devices. All of the difficulties mentioned above may be overcome empirically in R&D programs only to come back to haunt production if their causes are insufficiently understood.

Recommendation: It is recommended that a program be established to determine the critical parameters in controlling dimensional and electrical characteristics of metal contacts on GaAs. This involves identifying reactions, and their dependency on temperature, pressure, GaAs surface conditions, etc. In this way the reactions can be taken into account and controlled in processing. The effect of these reactions (and other changes during processing) on electrical and dimensional properties must be established so that they can be controlled so as to insure production yields and reliability of the final IC.

Benefits: Lower costs (through higher yields) and more reliable GaAs ICs.

Issue: Non Au-Based Metallizations **Submitted By:** S. H. Wemple

Description: Au-based metallizations prevent utilization of Si-like fabrication techniques for GaAs ICs. Elimination of Au would increase compatibility between GaAs and Si wafer fabrication.

Recommendation: Increase wafer fabrication compatibility between GaAs and Si IC lines.

Benefits: Higher volume, lower cost, higher yields.

Issue: Al-Metallization To Replace Au **Submitted By:** R. Zuleeg

Description: Energy absorption from x-ray radiation yields for the AuGe system has a value of 14 cal/g to reach the eutectic temperature and melt the IC ohmic contacts. This is not acceptable for radiation hardened circuitry for SDI radiation environments. A feasible system to replace the AuGe system is AlGe. This system can stand 146 cal/g heat absorption before it will melt. It, therefore, constitutes a viable system for radiation hardened GaAs ICs in analogy to Si IC technology.

Recommendation: Develop AlGe ohmic contact technology for GaAs IC technology and Al interconnect techniques for first and second level. Utilize the expertise of dry etching Al interconnects in the application to GaAs IC fabrication.

Benefits: Acquisition of radiation hardened GaAs ICs for SDI application. Reduction of price by replacing Au with Al. More reliable and temperature stable ICs.

Issue: Interconnect Capacitance Reduction **Submitted By:** S. H. Wemple

Description: Parasitic interconnect capacitances limit the speed of LSI/VLSI circuits. Multi level and/or airbridge schemes may be devised which would reduce this speed-limiting parasitic.

Recommendation: Development of low dielectric constant multi-level interconnects for GaAs ICs.

Benefits: Higher speed and lower power.

Issue: Low Cost FET/MIMIC Technology **Submitted By:** R. W. Bierig

Description: Present MESFET and MIMIC fabrication technology and design procedures suffer from relatively high cost because of only a few technology drivers. The use of "backside" thinning and processing is driven by the need to minimize the amount of GaAs between heat source and heat sink because of the poor thermal conductance of GaAs. This process (thinning) has performance implications primarily for devices with dissipation levels of 1W/mm or higher. Gate recessing provides enhanced FET performance over what can be generally obtained from surface gates. However, the gate recessing process is a source of significant cost, performance non-uniformity and process "artistry". A fully planarized gate formation process without performance degradation is needed. For many MMIC applications (principally low power) a co-planar design format offers substantial cost advantage over a microstrip approach. Current CAD has few co-planar circuit models to support any but trivial designs.

Recommendation: Eventual development of epitaxy on high thermal conductance substrates will reduce the need for a "back side" process. However, significant cost savings can be realized by supporting co-planar designs for low power applications. There are two program elements recommended: (a) a non-recessed, higher performance gate process, and (b) development of co-planar circuit and device models. Program (a) should incorporate a study of GaAs surface physics, surface stabilization, high quality channel formation using surface gates. Program (b) will require about equal amounts of device fabrication and characterization; model development and verification. Program (a), 2 years - $800K; Program (b), 2 years - $1.5M.

Benefits: Program (a): yield increase in FET and MMIC fabrication; Program (b): a compatible technology to combine analog and digital functions on a single chip and a low cost fabrication process for low power MMICs.

Issue: High Throughput Sub-Half-Micron Lithography **Submitted By:** T. A. Midford

Description: The cost effective manufacture of high performance GaAs digital IC and MIMIC devices is, or will be, dependent of high throughput submicron production lithography. Current approaches (mostly laboratory) include: (1) contact optical or deep UV, (2) step on wafer (DSW), (3) direct write E-beam (or ion beam), and (4) X-ray lithography. In some instances, hybrid combinations of two of these technologies may be used, e.g., DSW and direct write E-beam. Direct write approaches offer maximum flexibility and greatest resolution but have throughput limitations, some of which have been addressed on VHSIC. The minimum linewidth achievable with DSW (probably the preferred production approach) is limited by the illumination wavelength.

Recommendation: Identify one or more approaches to high throughput, high precision production lithography for sub-half micron resolution. Define and develop necessary equipment at appropriate vendor(s). Install and validate equipment in one or more GaAs lines.

Benefits: Ability to economically produce high performance submicron GaAs parts.

Issue: In-Situ Processing for High Performance GaAs Devices **Submitted by:** J. S. Harris

Description: As the geometry of GaAs devices continues to decrease, surface effects create ever greater parasitics. Many of the new and proposed devices involve super lattices and quantum wells. These devices will require lateral patterning and the ability to make electrical contact to only a single epitaxial layer in a quantum well. If next generation devices are to be realized, they will require dimensional control and processing spatial resolution on the 100 Å scale. What is already known about the adverse effects of exposing GaAs surfaces to air and the dimensions of these new devices suggest that a complete in-situ or maskless processing technology must be developed to be successful in realizing many of the goals for quantum well devices.

Recommendation: Develop in-situ processing techniques for both MOCVD and MBE which include: surface cleaning for regrowth and multiple epi depositions, localized epitaxy and etching, metal deposition, doping and disordering with focused ion beam, insulator deposition, in-situ patterning for semiconductors, insulators and metals, etc. Recommended programs should involve substantial funds for development of new research equipment for in-situ processing.

Benefits: Develop fundamental materials and processing technology for next generation quantum devices. Should also have significant impact on current MESFET ICs, MODFETs, etc. for reliability and control over surfaces. The Japanese clearly made the first step in this area with development at OJRL.

Issue: Packaging for GaAs Digital And Analog Circuits **Submitted By:** C. G. Kirkpatrick

Description: Commercial packages offering high pin-out, thermal matching, and impedance control for GaAs digital devices are not available. Although some announcements of products have been made, actual delivery of these packages has not followed. Much of the tooling for specialized packages is also closed to other users. In analog GaAs, the situation is even more serious, with very expensive, labor-intensive fixturing required for these circuits.

Recommendation: Two program objectives need to be addressed, for digital and for analog GaAs devices. One involves the digital packaging issues alluded to above. The second involves focus on packages for MMIC testing, and MMIC final fixturing.

Benefits: The benefit to DoD from this activity is the actual ability to use higher performance GaAs parts, and get that advantage in the system application.

TESTING AND CHARACTERIZATION ISSUES

TITLE	AUTHOR
Ultra-High Speed Testing	J. S. Harris
On-Wafer RF And High Speed Digital Testing	T. A. Midford
High Speed (Low Cost) FET and MMIC Characterization	R. W. Bierig
High Speed Testing	P. A. Congdon
High Speed Testing	S. H. Wemple
Reliability Of GaAs Devices	C. G. Kirkpatrick
Solid State Device Failure Analysis	R. W. Bierig

TESTING AND CHARACTERIZATION

Issue: Ultra-High Speed Testing **Submitted By:** J. S. Harris

Description: Both high speed IC testing and new techniques to probe internal nodes of high speed ICs are severely lacking. Currently, all IC operational tests are done at well below operational speed. At the development end, the lack of ability to probe circuits greatly inhibits the development of large scale integration and accurate design models for high speed GaAs ICs. It makes correction of design and processing problems impossible.

Recommendation: Develop testing at 2 levels: 1) High speed digital and microwave testing of packaged ICs and devices at much lower cost and higher throughput, and 2) Exhaustive, internal node, probe level IC test techniques and equipment for development of ICs and design models to move up the integration level.

Benefits: Testing capability for all DoD high speed IC manufacturers.

Issue: On-Wafer RF And High Speed Digital Testing **Submitted By:** T. A. Midford

Description: Functional testing is a major cost adder for RF and digital circuits, in addition to being a major technical challenge. At present, most functional testing is performed after dicing in packages or on carriers which degrade overall device performance, usually to an unknown degree. With increasing frequency, mechanical uncertainties associated with package assembly tolerances become a major source of measurement error. Precision on-wafer testing can alleviate some of these problems, and in addition, provide a significant means to long term cost reduction.

Recommendation: Establish test procedures including required hardware and software for the on-wafer testing of GaAs RF (MIMIC) and digital circuits to a frequency of 100 GHz. Examine all feasible approaches including extensions of current technology (e.g., coplanar contacting problem systems) non-contacting approaches and integrated optical test structures.

Benefits: Cost reduction and improved performance of a wide variety of high performance parts.

Issue: High Speed (Low Cost) FET and MMIC Characterization **Submitted by:** R. W. Bierig

Description: Even with today's technology, techniques available for characterizing analog devices and MMICs are totally inadequate for device/component development and

production. Simple MMICs are being fabricated today with DC screen yields in the range 20%-50%, providing 100-300 die/wafer. Wafer fabrication cost is in the range $2K-$5K/wafer. Die mounting, die characterization and data analysis costs are approximately $100-$200/die not including test fixture or package cost. Complicated MMICs can be made with yields in the range 5%-15%; providing 10-30 die/wafer; assembly cost is similar to simple devices, but characterization can be a multi-day procedure costing $500-$15K/die. Very few (none to date) programs support complete characterization of all yielded devices with the result the customer/developer and technical community have accumulated very little of the available knowledge from the investment made. Yields are quoted at the "DC screen level" and little if any knowledge of correlation between DC screen parameters and RF performance exists.

Recommendation: Develop High Speed, Low Cost FET and MMIC characterization methods. The program should address analog and digital applications as well as device and component characterization for low noise and power generation requirements. It is anticipated the program will be a multi-company/university team effort and will take a dual path approach; (a) an evolutionary development starting with today's tech base and available equipment with defined augmentation over the contract term; (b) a revolutionary concept development/ evolution/implementation. Fund both (a) and (b) concurrently at ~ $2M/year for 3 years; projected funding split year 1 - 70% a, 30% b.; year 2 - 50% a, 50% b, year 3 - 30% a, 70% b.

Benefits: Much better return on investment in FET and MMIC development than is now possible. Substantial reduction in cost/unit in future device production.

Issue: High Speed Testing **Submitted By:** P. A. Congdon

Description: The majority of current IC testers satisfy silicon requirements:
clock frequency < 100 MHz, I/O Count < 200 (100 typically), and poor timing skew control. The time required to test complex parts is excessive in light of tester cost.

Recommendation: Develop a high speed test head and high pin count handler.

Benefits: Savings in time and cost.

Issue: High Speed Testing **Submitted By:** S. H. Wemple

Description: High-Speed multi-pin logic/memory testing is currently inadequate for GaAs ICs.

Recommendation: Exploration of the key design issues relevant to high speed testing including edge rates, cross talk, timing, skew, powering, and I/O circuitry.

Benefits: Performance and Cost.

Issue: Reliability of GaAs Devices **Submitted By:** C. G. Kirkpatrick

Description: The issue here is not just testing the youthful technologies in GaAs to determine reliability, yes or no, but determining the methods to improve the reliability of GaAs devices.

Recommendation: The program objective should focus on determining the failure mechanisms affecting the reliability of GaAs devices. These investigations should involve experimental and theoretical work, to measure and analyze the results. Experiments to try alternative processes and designs should follow, with another cycle of testing and analysis.

Benefits: The benefit to DoD will be accelerated usage of the GaAs technology in systems, and a higher reliability product base for applications.

Issue: Solid State Device Failure Analysis **Submitted By:** R. W. Bierig

Description: There has been no comprehensive assessment of design, material, fabrication processes, assembly procedures or operating voltages that impact solid state device reliability. No useful reliability models exist nor do guidelines to support reliability exist.

Recommendation: A three-year program of device failure analysis at a level of ~ $1M/ year. The program is to be managed by an industrial contractor, use devices from all available sources and employ the resources of government facilities for specialized test equipment.

Benefits: An industry wide III-V compound device reliability knowledge base.

NEW DEVICES AND APPLICATIONS ISSUES

TITLE	AUTHOR
Quantum Well and Superlattice Devices	P. C. T. Roberts
Heterojunction Bipolar Transistors	J. S. Harris
High Speed E-JFET Technology	R. Zuleeg
New GaAs Integrated-Optics Signal Processing	P. C. T. Roberts
Photonic Technologies and Systems	T. A. Midford
Optically Interconnected Computers	Karl Hess
GaAs Signal Processor for IR Focal Plane Arrays	T. A. Midford

NEW DEVICES AND APPLICATIONS

Issue: Quantum Well and Superlattice Devices **Submitted By:** P. C. T. Roberts

Description: Ability to grow quantum well and superlattice device structures opens up new quantum mechanical phenomena for use in advanced devices. Increased support of this area of research could lead to entirely new device approaches that may circumvent present speed, power and interconnect limitations.

Recommendation: Define new device structures based on supperlattices or quantum well structures which lead to unique high performance parameters not available in conventional devices. Quantum well tunnel devices are excluded.

Benefits: Higher performance devices.

Issue: Heterojunction Bipolar Transistors **Submitted by:** J. S. Harris

Description: HJBT are still being developed in only 2 or 3 research laboratories. Results on these devices, particularly in A/D and D/A conversion look extremely encouraging. There is only primitive IC technology, no CAD or circuit simulation capability. Simple models for HJBT suggest that at least a 10X increase in performance of A/D operations can be realized. There is, at present, only very limited HJBT research.

Recommendation: Increase level of support (there are 3-4 such programs) particularly with emphasis on self-aligned processing, device physics, device and circuit models and high speed characterization.

Benefits: A/D and D/A conversion are the time limiting and crucial link between the analog and digital worlds for signal processing, computer interfacing and control. An advance by 10X appears possible with HJBTs.

Issue: High Speed E-JFET Technology **Submitted By:** R. Zuleeg

Description: Existing E-JFET technology (standard approach) achieves at 200 μW/gate power dissipation at a switching speed of 150-200 ps. For high speed memory and micro-processor designs, i.e., 1 ns access time and 200 MHz clock rates, improved frequency response is required. The present structure of the E-JFET leads to good yield figures for LSI and VLSI circuit fabrication and it is expected that this high yield processing can be maintained also with a new high speed structure JFET.

Recommendation: Develop low-power, high speed GaAs E-JFET technology with self-aligned gate structure. This improvement in structural dimensions is aimed at 0.5 to 1.0 μm channel length and has prospects of 50 ps propagation delay times and 200 μW power dissipation. This performance offers VLSI potential and over 10,000 gates per chip with a 2 watt chip power dissipation limit.

Benefits: Radiation hardened ICs for space and military applications. LSI and VLSI parts not possible with Si technology.

Issue: New GaAs Integrated-Optics Signal Processing **Submitted By:** P. C.T. Roberts

Description: Several military systems are known to demand data manipulation/signal processing throughput rates which are ideally 100x faster than presently achievable. ARIADNE, for example, seeks to obtain a 20dB increase in target detection sensitivity. Fiber-optic gyros are another application where high accuracy, high sensitivity and, particularly, low cost would be essential for military use. Multi-sensor systems, where data is "fused" at ultra-high rates, is one more military application area.

Recommendation: Define new research to combine the fields of: systems architecture, circuit design (new principles), device structures using I-O. Develop implementation alternatives based on mostly-optical GaAs (or other compounds) devices.

Benefits: Very high system throughput at low cost and high reliability, serving multiple application areas.

Issue: Photonic Technologies and Systems **Submitted By:** T. A. Midford

Description: One of the principal advantages of III-V microelectronics is its compatibility with optics. A broad variety of system functions can be performed by a combination of microwave or millimeter wave, high speed digital and optical components, some or all of which may be monolithically integrated. A simple example is a microwave carrier on a fiber optic link. Such a system requires an integrated modulator/solid state laser driver, together with an integrated photodetector/ receiver. Considerable work remains to establish a compatible and manufacturable technology base for such "photonic" components.

Recommendation: Define and develop a manufacturable technology for photonic devices and components. Extend present microwave modulation techniques to millimeter wave frequencies. Demonstrate one or more complete photonic systems.

Benefits: Technology base for a wide range of new military components and systems, some of which are not available with current technologies.

Issue: Optically Interconnected Computers **Submitted By:** Karl Hess

Description: Short distance optical interconnections may be beneficial for future computers (especially supercomputers) on several levels: in between CPUs, in between circuit boards, in between chips and on future optoelectronic chips (the latter will need new device ideas; e.g., a device whose "gate" is sensitive to light).

Recommendation: To explore high speed optoelectronic sources and detectors (switching frequency larger than 10 GHz), the combination of Si - GaAs technology, optoelectronic pattern generation (such as interdiffusion of super lattices) and questions of packaging related to short distance interconnects.

Benefits: New generation of ultrafast optically interconnected supercomputers (not necessarily optical computers); ultrafast short distance optical communications.

Issue: GaAs Signal Processor for IR Focal Plane Arrays **Submitted By:** T. A. Midford

Description: Infrared (IR) detectors are important sensors for surveillance, discrimination, and tracking. In order to extract electrical signals from multiple detector focal plane arrays (FPA), low-power, high-data-rate, radiation hardened, low-noise, and high-density readout circuits are required, which operate in a cryogenic environment. Furthermore, some essential signal processing such as double sampling correlation and background subtraction, must be performed at the FPA and hence at cryogenic temperatures. Such signal processors require low-power and must be integratable with the FPA. GaAs has a good match in thermal expansion with some of the most popular IR detectors, such as HgCdTe and InSb. GaAs devices consume less power than Si and operate at higher speeds. GaAs MESFETs and HEMTs are hard up to a radiation dose of about 1.0E8 Rads. In addition, monolithically integrated electro-optic devices may be used in conjunction with fiber optics to output the signals from the focal plane dewer.

Recommendation: Develop high density GaAs MESFET or HEMT readout circuit arrays that can be hybrid interfaced with HgCdTe or InSb IR detector arrays. Develop FPA signal processors in conjunction with readout circuit arrays. Develop production units.

Benefits: High-performance, reliable, and radiation multiple FPA for surveillance, thermal imaging, missile systems.

PROGRAMMATIC ISSUES

TITLE	AUTHOR
Insertion Issues for GaAs Circuits	C. G. Kirkpatrick
Systems Applications	T. A. Midford
GaAs ICs and Pilot Lines	J. S. Harris
Centers of Excellence	R. W. Bierig
Radiation Hardness	D. R. Collins
Radiation Hardness	P. A. Congdon

PROGRAMMATIC ISSUES

Issue: Insertion Issues for GaAs Circuits **Submitted By:** C. G. Kirkpatrick

Description: At present, the high performance and circuit demonstrations in GaAs have resulted in a solution looking for a problem. The insertion of GaAs circuits and user acceptance for system applications are problems in its evolution, as are the technical development issues. A strong initiative in the area of GaAs insertion is critically needed for DoD's investment to reach fruition.

Recommendation: The program objective is the identification of near-term systems applications, assistance in addressing the issues for insertion into these systems, and actual demonstration of GaAs parts in systems.

Benefits: The benefits to DoD would involve more rapid acceleration of GaAs parts into system applications, and a larger base for usage, driving down costs.

Issue: Systems Applications **Submitted By:** T. A. Midford

Description: Although discrete GaAs field effect transistors are widely used, digital and/or monolithic circuits are not. There are many reasons why systems designers are reluctant to employ GaAs circuits. One of the dominant reasons appears to be that no one has done it yet. Thus, there is the proverbial "chicken and egg problem". This problem can be overcome if the risks involved are shared or shouldered entirely by the government. In a sense, the MIMIC program is a response to this situation. But MIMIC will be a success from a systems perspective, only if it addresses and reduces the risk of all elements of the system. Development of generic chips which address the so-called "critical elements" or "building blocks" are not sufficient since they will only partially demonstrate the viability of the system concept.

Recommendation: A sensible program would select a relatively simple EW or communications system and implement all of the necessary GaAs functions as part of a single program activity. This would ensure that a successful system would result if all the chips were fabricated. It would clearly demonstrate the viability of GaAs for systems applications.

Benefits: Successful demonstration of a full functional system based on GaAs components would encourage systems designers, both in industry and government, to employ the technology on a wider basis. To date, such demonstrations are lacking.

Issue: GaAs ICs and Pilot Lines **Submitted by:** J. S. Harris

Description: DARPA in particular, but US industry as well, have established a number of GaAs pilot lines which appear to be greatly underutilized. The problem appears to be multi-faceted, including: 1) lack of creative, innovative and risk taking systems designers, 2) lack of university programs focused on high speed design and systems to train people in this area, 3) high cost of current pilot lines, 4) problems of how to divide a system up between GaAs and Si and interfacing between them, 5) insufficient data base and manufacturing expertise in pilot lines and 6) lack of foresight on long-range potential and goals for GaAs.

Recommendation: Programs to stimulate use of pilot lines to: 1) develop design experience with GaAs, 2) investigate new high speed circuits and systems, architectures and 3) gain experience in production and learning curve for GaAs ICs. Programs should be established in universities to design high speed ICs, use pilot lines as foundries and test ICs to verify their designs. Programs in industry should initially focus on innovative designs and advances (like 32 bit RISC μP DARPA program) rather than immediate end use applications, but should also require multiple pilot line use rather than a single (usually in-house) fab facility. There is a need to educate users and underwrite part of the cost for using facility and reduce risk for user.

Benefits: Realize multiple sources for "real" GaAs ICs and develop a generation of circuit and systems designers and architects who are knowledgeable about both the advantages of GaAs and its limits and who design and utilize the technology accordingly.

Issue: Centers of Excellence **Submitted By:** R. W. Bierig

Description: 6.1 dollars invested in industrial research laboratories have relatively poor ROI because industrial management emphasizes relatively short term solutions. 6.1 dollars invested in university labs have relatively poor ROI because university management has no schedule orientation or application base. 6.1 dollars invested in DoD facilities serve primarily to sustain a knowledge base without significant stimulation of 6.2 programs. What is needed is a method to marry industrial management and needs knowledge with university level research and analysis depth and selective collaboration with DoD personnel. The concept proposed is to establish "centers of excellence" at approximately six locations throughout the U.S. The centers should be fully supported by DoD so there is no question about ownership of output and imposition of ITAR and EARs. Capital equipment and facilities should be government owned. Program management personnel should be drawn from industry and DoD where appropriate. Program participants should be solicited from local industry and university and DoD talent pools. The program success will be directly dependent on how industry perceives their "gain" from "investing" (leave of absence) talented personnel and how universities perceive they will expand their research opportunities. Industry will only relinquish talent if they can reasonably expect to get improved talent back at a future, but definite, time. University personnel will participate to the extent their opportunities to do something "new" are enhanced. Both desires

can be met in a single environment with proper planning and support. (I think the "Diamond Initiative" being discussed for establishment at Triangle Research would be much more attractive to industry (and DoD) if proven industrial (or other) management skills (talent) were proposed for program direction. Without proper management and a mix of both short term as well as long-term goals, the program appears unattractive.) I think it is relatively unlikely that industry or DoD will supply their best talent to a technology program unless the term is finite and fixed and unless the personnel can maintain their home environment. I think the research funds now invested in establishments such as Lincoln Labs, Triangle Research Institute, NOSC and many others I don't know could be better used if there was both an industrial representation and DoD representation. I think the 6.1 dollars invested in industry could provide much higher technological growth leverage if they were invested in "cross-pollinated" facilities.

Recommendation: To establish centers of excellence throughout the U.S. to augment the efficiency of investment in emerging or speculative technologies of national interest. A single center should be interdisciplinary but not necessarily comprehensive. Nominal recommendation for centers in Boston, Washington, Atlanta, Chicago, Denver, Dallas, San Diego - Los Angeles, San Francisco, Seattle at existing government facilities is recommended. Phase 1 is to be 12 months to define location missions and facilities. Phase 2 is for 12 months to define initial programs and initial staffing and budget requirements.

Benefits: At little or no increase in cost, DoD can increase ROI in 6.1 funding.

Issue: *Radiation Hardness* **Submitted By:** D. R. Collins

Description: Many military applications require operation in high radiation environments. Most systems do not respond to this need because the components do not exist with proper radiation hardness, and so the system requirements are down-scoped to avoid development "risk." The silicon community, in general, protects their position and will not advocate radiation hardness requirements that exceed silicon capability.

Recommendation: Develop a standard family of GaAs devices - logic, memory, and linear which will provide increased levels of radiation hardness. There will be a trade-off between complexity/availability and hardness. The goal would be to have a set of interchangeable parts which could be supplied by a number of companies to the DoD community.

Benefits: Family of progressively more radiation hard devices for general system use.

Issue: Radiation Hardness **Submitted By:** P. A. Congdon

Description: Achievement of strategic radiation tolerance levels is not possible with most existing technologies without performance degradation. Many radiation hardening approaches adversely impact circuit density and yield.

Recommendation: Have multiple contractors fabricate a government defined test circuit and evaluate radiation tolerance. Concentrate improvement effort on most promising technology.

Benefits: Improved rad-hard circuits.

GLOSSARY OF TERMS

A/D	analog to digital
Al	aluminum
AlGe	aluminum-germanium
As	arsenic
Au	gold
AuGe	gold-germanium
CAD	computer aided design
CMOS	complimentary metal oxide semiconductor (silicon technology)
CPU	central processing unit
D/A	digital to analog
DC	direct current
DLTS	deep level transient spectroscopy
D-MESFET	depletion metal semiconductor FET
DSW	direct step on wafer
EAR	export administration regulation
E-beam	electron beam
E/D-MESFET	enhancement/depletion metal semiconductor FET
E-JFET	enhancement junction field effect transistor
EL2	midgap electron trap in GaAs
EPD	etch pit density
ESCA	electron spectroscopy for chemical analysis
EW	electronic warfare
FET	field effect transistor
FPA	focal plane array
GaAs	gallium arsenide
GHz	gigaHertz, 1E9 Hertz
HBT	heterojunction bipolar transistor
HEMT	high electron mobility transistor
HgCdTe	mercury cadmium telluride
HJBT	heterojunction bipolar transistor
IC	integrated circuit
III-V	column 3 and column 5 of the periodic table
IR	infrared
ITAR	international traffic in arms regulations
JFET	junction field effect transistor
LEC	liquid encapsulated Czochralski
LED	light emitting diode
LPE	liquid phase epitaxy
LSI	large scale integration
MBE	molecular beam expitaxy
MHz	megaHertz, 1E6 Hertz
MIMIC	millimeter and microwave integrated circuit
MMIC	monolithic microwave integrated circuit
MOCVD	metalorganic chemical vapor deposition; also called MOVPE
MODFET	modulation doped FET, also called HEMT or TEGFET

MOVPE	metalorganic vapor phase epitaxy
NMOS	n-channel metal oxide semiconductor
OJL	Optical Joint Laboratory (in Japan); also called OJRL
OJRL	Optical Joint Research Laboratory
PIS	photo-induced spectroscopy; also called PITS
PITS	photo-induced transient spectrometry
PL	photoluminescence
R&D	research and development
RF	radio frequency
ROI	return on investment
SDI	strategic defense initiative
Si	silicon
SIMS	secondary ion mass spectroscopy
TEGFET	two-dimensional electron gas FET
T/R	transmit/receive
VHSIC	Very High Speed Integrated Circuit
VLSI	very large scale integration
VPE	vapor phase epitaxy
watt	microwatt, 1E-6 watt

III-V MICROELECTRONICS PANELISTS

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